REMARKS/ARGUMENTS

I. Introduction

This amendment is respectfully submitted in response to the Office Action dated August 17, 2004. The amendment follows a December 9, 2004 telephone interview summarized below. Applicants thank the Examiner for the opportunity to discuss the application during the telephone interview.

Claims 1-26 are pending. Claims 16 and 25, which the Examiner indicated were directed to allowable subject matter have been rewritten in independent form. In addition claims 1, 3-6 and 11-26 have been amended to address and overcome the Examiner's objections to various claims and to clarify the claims.

In addition to amending the claims, Applicants have amended the specification to correct minor numbering and grammatical errors. The amendments to the specification are supported by the figures and text found in the application as filed.

In the Office Action the Examiner objected to claims 1, 3, 5, 6, 11 and 12 because of various informalities discussed on page 2 of the Office Action. In addition, the Examiner rejected claims 4, 6 and 13-26 as being indefinite because of the wording issues raised by the Examiner. As will be discussed below, Applicants have amended the claims to address and overcome these rejections.

With regard to prior art, the Examiner rejected claims 1-10, 13-15 and 17-24 under 35 U.S.C. §103 as being unpatentatable over U.S. Patent No. 5,864,703 to van Hook et al (hereinafter van Hook '703) in view of U.S. Patent No. 5,933,650 to van Hook et al (hereinafter van Hook '650). Claims 11 and 12 were rejected under 35 U.S.C. §103(a) in view of the van Hook patents when considered in combination with U.S. Patent No. 6,754,804 to Hudepohl et al. (the Hudepohl et al. patent).

II. Interview Summary

This interview summary is presented in the format suggested by the Patent Office. Note that Tom Richardson, one of the inventors, participated in the telephone interview and has been included on the list of participants although he was apparently left off the Examiner's interview summary record by what appears to be a minor oversight.

1. **Application Number: 10/618,325**
2. **Name of Applicant: Hui Jin et al.**
3. **Name of Examiner: Stephen M. Baker**
4. **Date of Interview: December 12, 2004**
5. **Type of Interview:** Telephonic
6. **Name of Participants:**
   Examiner: Stephen M. Baker;
   Applicants' Rep: Michael P. Straub
   Inventors: Hui Jin, Tom Richardson
7. **Exhibit(s) Shown:** None
8. **Claims discussed:** Pending claims 1-26 were discussed.
9. **Prior Art Discussed:**

U.S. Patent Nos. 5,864,703; 5,933,650 and 6,754,804

10. Proposed Amendments discussed:

Applicants discussed amending various claims to focus on the LDPC aspect of the invention and to indicate that the reordering were supported at a bit level and not in multi-bit subportions.

11. Discussion of General Thrust of the Principal Arguments

Applicants argued that the van Hook patents as well as the other applied reference did not discuss or disclose LDPC encoding or methods or apparatus for performing such encoding. It was further argued that the van Hook patents were clearly directed to selecting and routing multi-bit portions of input values and that the shuffle networks cited in the van Hook patent did not perform bit level reordering on an input value and then output the full, but re-ordered value.

12. Other Pertinent Matters Discussed:

The Examiner identified some numbering errors in the specification with regard to references to the figures and suggested that Applicants review the specification and amend it to correct any errors in the reference to various figures. Applicants agreed to review and amend the specification to clarify it.

13. General Results/Outcome of Interview

The Examiner indicated he would review Applicants formal written response to the Office Action upon its submission.

III. The Claim Objections Have Been Overcome

Claims 1, 3, 5, 6, 11 and 12 were objected to for the reasons set forth on page 2 of the office action.

With regard to claim 1, line 7, the Examiner objected to "passing computed". Applicants have amended claim 1 to replace this phrase with "passing the computed" which is appropriate.

With regard to claim 3, line 3, Applicants have amended the claim to recite "the reordering for" which is consistent with the Examiner's suggestion but with "reordering" being used instead of switching to be consistent with the other revisions to claim 3.

With regard to claim 5, "order of" has been changed to "order the" as suggested by the Examiner.

With regard to claim 6, the claim has been amended to depend from claim 5 instead of claim 2. In view of the amendment, it is believed that the claim dependency is now correct.

With regard to claim 11, "claim 2" has been changed to --claim 4-- as suggested by the Examiner.

With regard to claim 12, "device" has been changes to --module-- as suggested by the Examiner.

In view of the above discussed amendments, it is respectfully submitted that the objections to the claims have been overcome.

In the Office Action the Examiner indicated that claims 16, 25 and 26 would be allowable if rewritten to overcome the rejection under 35 U.S.C. §112, 2nd paragraph. Applicants thank the Examiner for this indication of allowable subject matter and have rewritten claims 16 and 25 in independent form while also amending the claims to address the §112 issues. In view of the amendments, newly independent claims 16 and 25 are in condition for allowance. Claim 26 depends from claim 25 and is therefore in condition for allowance for the same reasons claim 25 is allowable.

In the Office Action the Examiner objected to claims 1, 3, 5, 6, 11 and 12 because of various informalities identified in the Office Action. In addition, the Examiner rejected claim 4, 6 and 13-26 under 35 U.S.C. §112, second paragraph as being indefinite because of working found in claims 4, 6, 13, 17, 24, 18 and 24 as discussed on page 3 of the Office Action.

As will be discussed below, in view of the amendments to the claims, each of the objections and rejections have been overcome.

IV. The §112, Second Paragraph Rejections Have Been Overcome

Claim 4, 6 and 13-26 were rejected as being indefinite. In the Office Action the Examiner states:

In claims 4, 6, 13, 17, 24 and 26 … it is not clear whether application is using "rotation" and "rotated" synonymously with "permutation" and "permuted".

Applicants have amended the claims so that "rotation" and "permutation" are not used in the claims. It is respectfully submitted that the "reordering" language used in the pending claims is definite and supported by the specification. **In view of the amendments to the claims to remove the "rotation" language and the fact that the claims do not use "permutation" it is respectfully submitted that the claims are definite.**

V. Claims 16 and 25-26 Are In Condition For Allowance

In the Office Action the Examiner indicated that claims 16 and 25-26 were directed to allowable subject matter and would be allowed if amended to overcome the §112, second paragraph rejections. **Applicants have amended claims 16 and 25 so that they are now in independent form and are definite. Claim 26 depends from allowable claim 25. Accordingly, it is believed that claims 16, 25 and 26 are now in condition for allowance.**

VI. The Prior Art Rejections Have Been Overcome

1. General Discussion of The Prior Art Rejections

In the Office Action, the Examiner relied primarily on the combination of the van Hook '703 and '650 patents to reject the claims. Both of the van Hook patents are directed to various SIMD processing operations none of which teach, disclose or suggest the claimed subject matter.

As discussed during the telephone interview, in contrast to the applied references, the methods and apparatus of the present invention are directed to methods and apparatus which are directed to performing Low Density Parity Check (LDPC) encoding operations. **The van Hook patents do not mention LDPC encoding, let alone the particular LPDC methods and apparatus to which the pending claims are directed.** Furthermore, the shuffle networks described **in van Hook which are used in the context of SIMD processing are not directed to apparatus for performing bit level reordering operations but are intended to deal instead in multi-bit portions.**

Applicants have amended the claims to more distinctly claim Applicant's invention. In contrast to the shuffle network type operations described in the van Hook patents, the present invention is directed to an apparatus for performing encoding operations where Z-bit vectors which are passed between a vector unit processor which performs XOR operations, are subject to re-ordering operations, e.g., bit level reordering operations, as they are passed through a reordering device used to couple the memory and vector processing unit together. The reordering device reorders the elements of a Z-bit vector as it is passed through the reordering device. Thus, while the reordering device may rearrange the order of the bits which are the elements of the Z-bit vector, it does not alter the elements of the Z-bit vector by subsisting a portion of another vector for the bits of the Z-bit vector. Thus, **in accordance with the**

invention, the elements of the Z-bit vector remain the same but their order is changed.

In contrast to various embodiments in the van Hook patents, in accordance with the invention, the full set of Z-bit vector bits received at the reordering device's input are, in accordance with the invention, passed to the device's output. Thus, the reordering circuit performs a reordering operation on at least one Z-bit vector rather than selecting a subset of the input followed by the routing of the subset to a different destination than say, some other portion of the Z-element input vector.

In contrast to the present invention, in both the van Hook patents it is clear that the elements of each vector which are being processed are **multi-bit** elements where a vector may include one or more multi-bit elements. See for example, the van Hook '703 patent col. 1, lines 20-24 which discuss 8, 12, 13, 24 bit numbers and the discussion of 16 bit data elements which are used in a processor with a 64 bit width (col. 1, lines 49-56) Furthermore, the summary of the van Hook '703 patent makes it clear that each data element is N bits in width and that the invention of the '703 patent involves loading a set of N bit elements into a vector register. (Col. 2, lines 47-61) Similarly, it is clear from the van Hook '650 patent that the data elements which can be stored in a vector register are each multi-bit units. See, e.g., col. 5 lines 55-65 of the '650 patent which states "The present invention allows data types of 8-,

16-bit, 32-, or 64-bit fields. Hence, a 64 bit doubleword vector may contain 8 8-bit elements, 4 16-bit elements, 2 32-bit elements or 1 64-bit elements. …"

In the van Hook patents neither of the references disclose a cross bar circuit which operates in the manner as the claimed reordering circuit recited in various pending claims.

In the Van Hook '703 patent it is clear that the disclosed crossbar is used for outputting all the elements, where each element is multiple bits, of a vector **without modification** or is used to select an element of the vector and to replicate it in the output. The van Hook '703 patent states:

> To perform arithmetic operations on desired elements of a vector, the present invention uses a well known crossbar method adapted to select an element of the vector register, vt, and replicate the element in all other element fields of the vector. That is, an element of vt is propagated to all other elements in the vector to be used with each fo the elements of the other vector operand. Alternatively, all the elements of the vector, vt, may be selected without modification. … (van Hook '703 patent col 7, lines 23-31)

Both of the '703 patents approaches teach away from the reordering of the present invention. Similarly, the various operations described in the van Hook '650 patent do not disclose or render obvious the reordering device or operation recited in various pending claims. Consider for example, Figs. 8A through 8H and Figs. 10A-10H. In

none of the illustrated operations is a complete but reordered set of elements from vs or vt transferred to the register vd. Each of the illustrated operations involves element duplication or combining of data elements from different sources (vs and vt) to fill vd. Accordingly, the pending claims are clearly patentable over the applied references.

The van Hook '703 and '650 patents which are used in combination to reject various pending claims describe the use of cross bar circuits to implement shuffle operations. The shuffle operations depend on processing multi-bit portions of a larger input. Such operations involve selection of a multi-bit sub-portion of the input and routing of the selected sub-portion to a particular destination. This may be described as a split and route operation where the different multi-bit portions are routed, e.g., to different devices. In this way, in the Van Hook patents different **multi-bit portions** of the input can be routed to completely different destinations. **However, the van Hook circuits can not perform bit level reorderings where the individual bits of a single input value are reordered without changing the bit content of the input value.**

Accordingly, it should be appreciated that the use of the re-ordering device and the methods of the invention which involve bit level reordering operations are in no way anticipated or rendered obvious by the shuffle network type routing and selection devices described the Van Hook patents.

The Hudepohl et al. patent, which is cited as describing an "encoder control module", does not make up for the above discussed deficiencies of the van Hook patents. Accordingly, the pending claims remain patentable over the Examiner proposed combination of references.

In view of the above discussion it is respectfully submitted that, as amended, the pending claims are patentable over the applied references.

2. Claims 1-12 and 17-23 Are Patentable

Independent claim 1 has been amended to more distinctly claim the subject matter Applicants regard as the invention.

Various features which are believed to render amended claim 1 patentable are indicated in bold below. As amended, claim 1 is patentable because it recites:

> An apparatus **for performing low density parity check encoding operations**, the apparatus comprising:
>
> memory including a set of memory locations for storing L Z-bit vectors, where Z is a positive integer greater than one and L is a positive integer;
>
> a vector unit operation processor including a circuit **for performing Z parity calculations in parallel to compute a Z-bit vector, each bit of the computed Z-bit vector being generated by one of the Z parity calculations**, an accumulator for storing the computed Z-bit vector, and an output device for passing the computed Z-bit vector to said memory; and

> **a reordering device** coupled to the memory and to the vector unit operation processor, the reordering device for passing Z-bit vectors between said memory and said vector unit operation processor and **for performing a bit level reordering operation on elements of at least one Z-bit vector, in response to reordering control information**, as the at least one Z-bit vector is passed between said memory and said vector unit operation processor by said reordering device.

Claims 2-12 depend from claim 1 and are patentable for the same general reasons that claim 1 is patentable.

3. Claims 13-15 and 17-23 Are Patentable

Independent claim 13 has been amended to more distinctly claim the subject matter Applicants regard as the invention.

Various features which are believed to render amended claim 1 patentable are indicated in bold below. As amended, claim 13 is patentable because it recites:

> A method of performing low density parity check encoding operations, the method comprising:
>
> storing L Z-bit vectors in a memory device, where Z is a positive integer greater than one and L is a positive integer;
>
> reading one of said L stored Z-bit vectors from said memory device;
>
> **performing a bit level reordering of the bits in said read one of said Z-bit vectors**; and
>
> operating a vector unit processor **to perform a plurality of parity check combining operations in parallel** to combine the bits of the reordered Z-bit vector with a

Z-bit vector stored in said vector unit processor to generate a new Z-bit vector.

Claims 14-15 and 17-23 depend from claim 13 and are allowable for the same reasons that claim 13 is allowable.

VII. Conclusion

In view of the above amendments and remarks it is respectfully submitted that the pending claims are definite and not anticipated or rendered obvious by the prior art of record.

In the event that there are any outstanding issues which need to be resolved after the Examiner reviews this amendment, Applicants invite the Examiner to call Applicants undersigned representative to discuss and hopefully resolve any issues that may need to be addressed to place the Application in condition for allowance.

Respectfully submitted,

February 17, 2005

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